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<u>AMENDMENTS TO THE CLAIMS</u>

Listing of the claims:

Following is a listing of all claims in the present application, which listing

supersedes all previously presented claims:

1. (Currently Amended) An input circuit for receiving a first input signal and

for use with a first power supply and a second power supply that supplies a voltage of

absolute value less than an absolute value of the first power supply, the input circuit

comprising:

a first differential amplification circuit powered by the first power supply to

receive and amplify the first input signal and generate a second input signal;

a level shift circuit powered by the first power supply to shift voltage of the

second input signal and generate a shifted input signal, the level shift circuit including

an output terminal; and

a second differential amplification circuit powered by the second power supply

to amplify the shifted input signal and generate an amplified signal;

a current control circuit connected between the first power supply and the first

differential amplification circuit to selectively switch the input circuit between an

activated state and a standby state,[[;]] and

wherein the level shift circuit further includes a first circuit for charging or

discharging voltage at the output terminal of the level shift circuit so that voltage of the

shifted input signal is less than or equal to the absolute value of the voltage of the

second power supply when switched to the standby state.

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2. (Original) The input circuit according to claim 1, wherein the first circuit

includes a constantly activated transistor.

3. (Original) The input circuit according to claim 1, wherein the first circuit

includes a transistor having a gate connected to the first power supply.

4. (Currently Amended) The input circuit according to claim 3, wherein the

first differential amplification circuit includes further comprising a second circuit for

charging or discharging a the voltage at an the output terminal of the first differential

amplification circuit when switching to the standby state.

5. (Original) The input circuit according to claim 4, wherein the second

circuit includes a constantly activated transistor.

6. (Original) The input circuit according to claim 4, wherein the second

circuit includes a transistor having a gate connected to the first power supply.

7. (Previously Presented) The input circuit according to claim 1, wherein

the level shift circuit further includes:

a level shift transistor having a drain connected to the first power supply and a

gate for receiving the shifted input signal; and

a load circuit connected between the level shift transistor and the first circuit to

adjust a level shift amount.

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8. (Currently Amended) An input circuit for receiving a first functional block

input signal and for use with first, second, third, and fourth power supplies, wherein

the second power supply supplies a voltage of absolute value less than an absolute

value of the first power supply, and the fourth power supply supplies a voltage of

absolute value less than an absolute value of the third power supply, the input circuit

comprising:

a first functional block including a first differential amplification circuit powered

by the first power supply and the second power supply, the first differential

amplification circuit receiving and amplifying the first functional block input signal to

generate a second functional block input signal;

a second functional block including a level shift circuit powered by the first

power supply and the second power supply to shift voltage of the second functional

block input signal and generate a third functional block input signal, the level shift

circuit including an output terminal;

a third functional block including a second differential amplification circuit

powered by the third power supply and the fourth power supply, the second differential

amplification circuit amplifying the third functional block input signal to generate an

amplified signal; and

a first current control circuit connected between the first power supply and the

first differential amplification circuit to selectively switch the input circuit between an

activated state and a standby state,[[;]] and

wherein the level shift circuit further includes a first circuit for charging or

discharging voltage at the output terminal of the level shift circuit so that voltage of the

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third functional block input signal is converged to a voltage between that of the third

power supply and that of the fourth power supply.

9. (Original) The input circuit according to claim 8, wherein the absolute

value of a potential difference between the first power supply and the second power

supply is greater than the absolute value of a potential difference between the third

power supply and the fourth power supply.

10. (Original) The input circuit according to claim 9, wherein each of the

second and fourth power supplies is a ground power supply that charges or

discharges the voltage at the output terminal of the level shift circuit when switching to

the standby state.

11. (Original) input circuit according to claim 8, further comprising an

additional circuit for charging or discharging the voltage at an output terminal of the

first differential amplification circuit when switching to the standby state.

12. (Original) The input circuit according to claim 8, wherein the first and

second differential amplification circuits and the level shift circuit each includes a

transistor having a gate oxidized film, wherein the gate oxidized film of the transistor in

the second differential amplification circuit is thinner than the gate oxidized films of the

transistors in the first differential amplification circuit and the level shift circuit.

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13. (Previously Presented) The input circuit according to claim 8, wherein

the first and second differential amplification circuits and the level shift circuit each

includes a transistor, wherein the withstand voltage of the transistor in the second

differential amplification circuit is lower than the withstand voltage of the transistors in

the first differential amplification circuit and the level shift circuit.

14. (Original) The input circuit according to claim 8, wherein the first current

control circuit includes a transistor having a gate for receiving a current control signal

that cuts the supply of power from the first power supply to the first differential

amplification circuit when switching to the standby state.

15. (Original) The input circuit according to claim 14, wherein the first

differential amplification circuit includes: a first pair of transistors, each having a type

of conductivity differing from that of the transistor in the first current control circuit and

having a gate for receiving the first functional block input signal; a load circuit

connected between the transistors of the first pair and the first current control circuit;

and a first current source configured by a transistor having a type of conductivity that

is the same as that of the first pair of transistors and connected between the

transistors of the first pair and the second power supply, wherein the transistor of the

first current source has a gate supplied with voltage that constantly activates the

transistor.

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16. (Original) The input circuit according to claim 15, wherein the load circuit

includes a current mirror circuit comprising a second pair of transistors, each being a

transistor having a type of conductivity differing from that of the first pair of transistors.

17. (Original) The input circuit according to claim 15, wherein the load circuit

includes a second pair of transistors, each having a type of conductivity differing from

that of the first pair of transistors and having a gate and a drain, the gates of the

second pairs of transistors being connected to the drains of the other ones of the

second pair of transistors.

18. (Original) The input circuit according to claim 15, wherein the load circuit

includes a pair of transistors, each having a type of conductivity differing from that of

the first pair of transistors and having a gate connected to the second power supply.

19. (Original) The input circuit according to claim 15, wherein the load circuit

includes a pair of resistors, each being connected in series to one of the first pair of

transistors.

20. (Original) The input circuit according to claim 14, wherein the first

differential amplification circuit includes: a first pair of transistors, each having a type

of conductivity that is the same as that of the transistor in the first current control

circuit and having a gate for receiving the first functional block input signal; and a load

circuit connected between the first pair of transistors and the second power supply.

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21. (Original) The input circuit according to claim 20, wherein the first

current control circuit functions as a current source of the first differential amplification

circuit when the input circuit is in an activated state.

22. (Previously Presented) The input circuit according to claim 14, wherein

the level shift circuit further includes:

a level shift transistor having a drain connected to the first power supply and a

gate for receiving the second functional block input signal, wherein the first circuit

includes a current source connected between the level shift transistor and the second

power supply and the current source of the first circuit comprises:

a transistor having a type of conductivity that is the same as that of the level

shift transistor, the transistor of the current source having a gate supplied with a

voltage that constantly activates the transistor.

23. (Original) The input circuit according to claim 22, further comprising a

second current control circuit connected between the level shift transistor and the first

power supply, wherein the second current control circuit cuts the supply of power from

the first power supply to the first level shift circuit when switching to the standby state.

24. (Original) The input circuit according to claim 23, wherein the second

current control circuit includes a transistor having a type of conductivity that is the

same as that of the transistor in the first current control circuit and of which is

responsive to the current control signal.

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25. (Original) The input circuit according to claim 22, further comprising a

third current control circuit connected between the second power supply and a node

between the first amplification circuit and the level shift circuit, wherein the third

current control circuit charges or discharges voltage at an output terminal of the first

differential amplification circuit when the first functional block input signal is not

received.

26. (Currently Amended) The input circuit according to claim 25, wherein

the first current control circuit includes a transistor, and the third current control circuit

includes a transistor having a type of conductivity differing from that of the transistor of

the first current control circuit, the transistor of the third current control circuit including

a drain connected to the output terminal of the first differential amplification circuit and

the gate of the level shift transistor, a source connected to the second power supply,

and a gate for receiving the current control signal.

27. (Original) The input circuit according to claim 22, wherein the level shift

circuit further includes a load circuit connected between the level shift transistor and

the current source to adjust a level shift amount.

28. (Original) The input circuit according to claim 27, wherein the load circuit

includes a diode-connected transistor.